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THE APPLICATIONS TECHNOLOGY SATELLITE IMAGE DISSECTOR CAMERA EXPERIMENT

by G. A. Branchflower, R. H. Foote, and D. Figgins

Goddard Space Flight Center
Greenbelt, Md.

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ABSTRACT

This paper describes the Image Dissector Camera experiment which is scheduled to fly aboard the Applications Technology Satellite-C. Camera system parameters are presented and a description of system operation, including the clock synchronizer and timing and control logic, is given. Ground support equipment is also discussed.

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THE APPLICATIONS TECHNOLOGY SATELLITE IMAGE DISSECTOR CAMERA EXPERIMENT

by

G. A. Branchflower, R. H. Foote*, and D. Figgins*

Goddard Space Flight Center

INTRODUCTION

The Image Dissector Camera (IDC) experiment described in this paper will be flown aboard the synchronous-orbit, spin-stabilized Applications Technology Satellite-C (ATS-C). The objective of the ATS-C experiment is the real-time transmission of daylight cloud cover information from the major portion of the full earth disk. The camera is a single package unit containing all the circuitry required to transform visual inputs into a composite electrical output containing both video and synchronizing information. Figure 1 illustrates the camera coverage.

Figure 1–Camera field of view.

SYSTEM DESCRIPTION

The IDC is completely electronic except for a protective shutter that closes over the face of the tube when the camera is not operating. The unit uses approximately 230 integrated circuit flat packs and 1000 discrete components. The major portion of the circuitry is contained on 21 plug-in-type printed circuit boards. The unit also includes two dc-to-dc converter modules, a voltage-controlled crystal oscillator, a sun sensor, the tube-coil assembly, and the lens. The basic system parameters are listed in Table 1. Figure 2 is a photograph of the camera.

The camera will be mounted with its optical axis perpendicular to the satellite's and

*ITT Industrial Laboratories.

Table 1
Image Dissector Camera System List of Parameters.

Parameter	Value
Size	5 in. x 12 in. x 11 in. (including lens)
Weight	20 pounds (without nutation sens.)
Power	20 watts (without nutation sensor)
Line rate	1.6667 Hz (at 100 rpm)
Frame rate	13.3 minutes (at 100 rpm)
Video baseband	28 KHz (at 100 rpm)
Composite wideband output	< 100 KHz (at 100 rpm)
Resolution	1328 TV lines
Field-of-view	14.6° (on a side)
Ground coverage	6040 x 6040 n.m.
Ground resolution at subsatellite point at zenith	 3.8 n.m. 7.5 n.m.
Zenith angle	57.53°
Signal-to-noise	40 db (at 10,000 ft lambert)
Iris	Fixed
Number of commands	12
Number of telemetry points	25

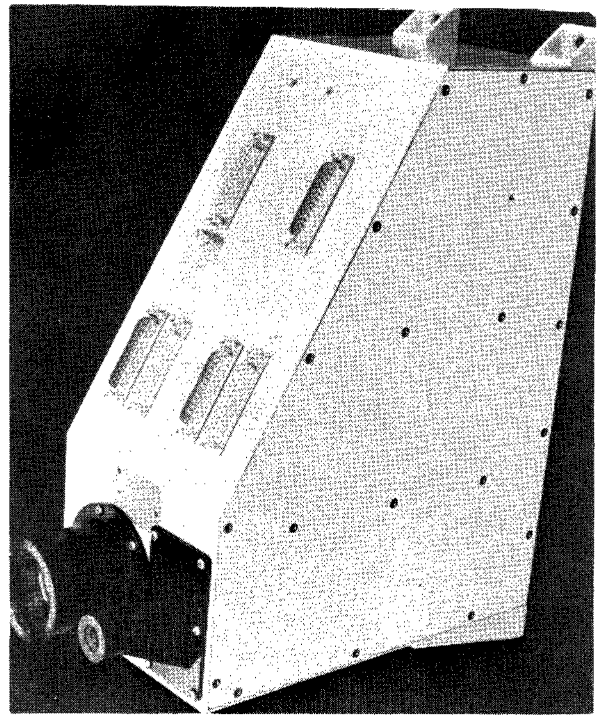

Figure 2—Photograph of camera.

earth's rotational axes. The camera's optical axis will trace a path on the earth from west to east as the satellite rotates. Application of proper deflection signals makes the camera scan a progression of lines, one per satellite rotation, until a complete raster is generated. In the primary mode of operation, scan lines on the earth will be traced parallel to the satellite spin axis. Ground commands initiate camera operation and select scanning mode. Table 2 shows a complete listing of camera commands and command functions.

Table 2
IDCS Command List.

Command	Function
Sec reg. off	Subsystem power completely off
Sec reg. on	Regulated 24-v power connected to camera
Camera off	Power to HF osc. and nutation sensor only
Camera on	Low voltage pwr supply on, clock synchronizer operating
Frame start auto	Camera operational with pictures taken automatically with from 1.41 to 2.82 minutes between pictures
Frame start manual	Camera operational for one picture then system returns to camera on state
Frame stop	Returns system to camera on state
Longitudinal mode	Primary scanning mode - camera line scans north to south
Latitudinal mode	Secondary scanning mode - camera line scans west to east
Look angle adjust quad	Picture phasing at 90° per command
Look angle adjust coarse	Picture phasing at 10° per command
Look angle adjust fine	Picture phasing at 22 minutes of arc per command

SYSTEM SCANNING MODES

In the primary or longitudinal scanning mode the camera sweep deflection provides line scan, and satellite spin supplies motion for vertical displacement. The line scan for this operating mode is north to south. Line scan in this direction is attained by supplying derotational deflection in the camera to counteract the effects of satellite spin, as well as the main deflection parallel to the satellite spin axis. Vertical or east-west displacement is achieved by initiating successive line scans slightly more slowly than satellite spin. That is, the time between the initiation of successive scans is the time the satellite takes to complete one full rotation plus the rotation that constitutes one scan line width. In this manner adjacent lines scanned across the earth are contiguous. Lines scanned as described above undergo displacement errors due to satellite spin axis nutation less than lines scanned in the direction of satellite rotation. Also, most errors that do occur in the presence of moderate spin-axis nutation can be corrected on the ground. Figure 3 illustrates the primary scanning mode.

In the secondary or latitudinal scanning mode, satellite spin motion provides line scan from west to east while the camera deflection signal supplies successive one-resolution element steps from north to south at the rate of one per spin until a complete raster has been obtained. If satellite spin-axis nutation is negligible (0.001 degree or less), the secondary scanning mode will produce pictures as good as those obtained in the primary scanning mode. Figure 4 illustrates this secondary scanning mode.

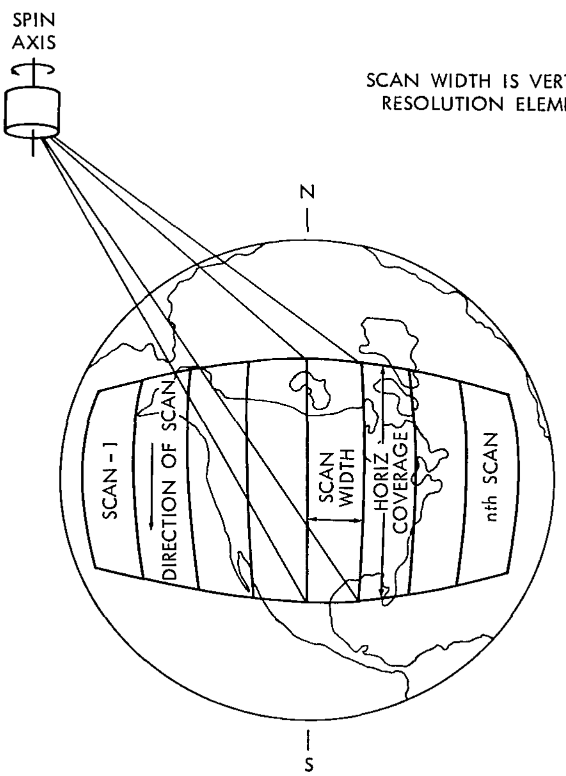

Figure 3—IDC primary scanning mode.

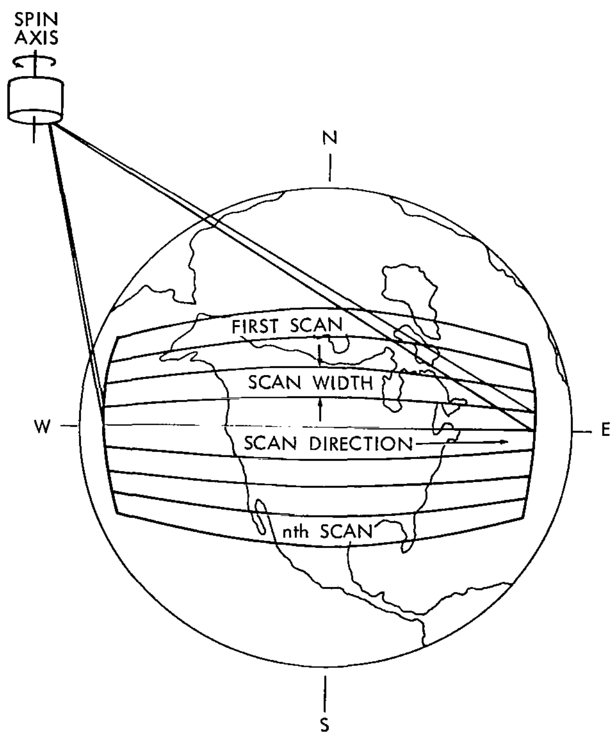

Figure 4—IDC secondary scanning mode.

CAMERA SYSTEM OPERATION

Figure 5 shows the general block diagram of the IDC. The sensor output is connected through a low-noise preamp to a low-pass filter, a black level clamp, and a buffer amplifier. The sensor video is then gated with frame sync, line sync, sun pulse, and nutation data to form the composite video signal. This composite signal is then used to amplitude-modulate the subcarrier signal derived from the system clock. This subcarrier amplitude-modulated signal is the system composite wideband output. The various components of this wideband output are shown in Figure 6.

The timing and control logic supplies the synchronization and gating necessary to properly phase the camera sweep deflection with satellite position and insert the components of the composite output signal into the proper timing sequence. One of the prime inputs to the control logic is the clock synchronizer output. The clock synchronizer maintains a system clock rate proportional to satellite spin rate over a range of 60 to 140 rpm. This clock signal, after proper shaping, is also used as the subcarrier signal for the system wideband output. The sun sensor supplies satellite spin rate data to the clock synchronizer; with a small achromatic lens it focuses the sun's image onto a strip of slot-masked solar cells. The output from these cells is coupled to a threshold detector, which incorporates an AGC loop, for rejection of lower-level signals. The detector

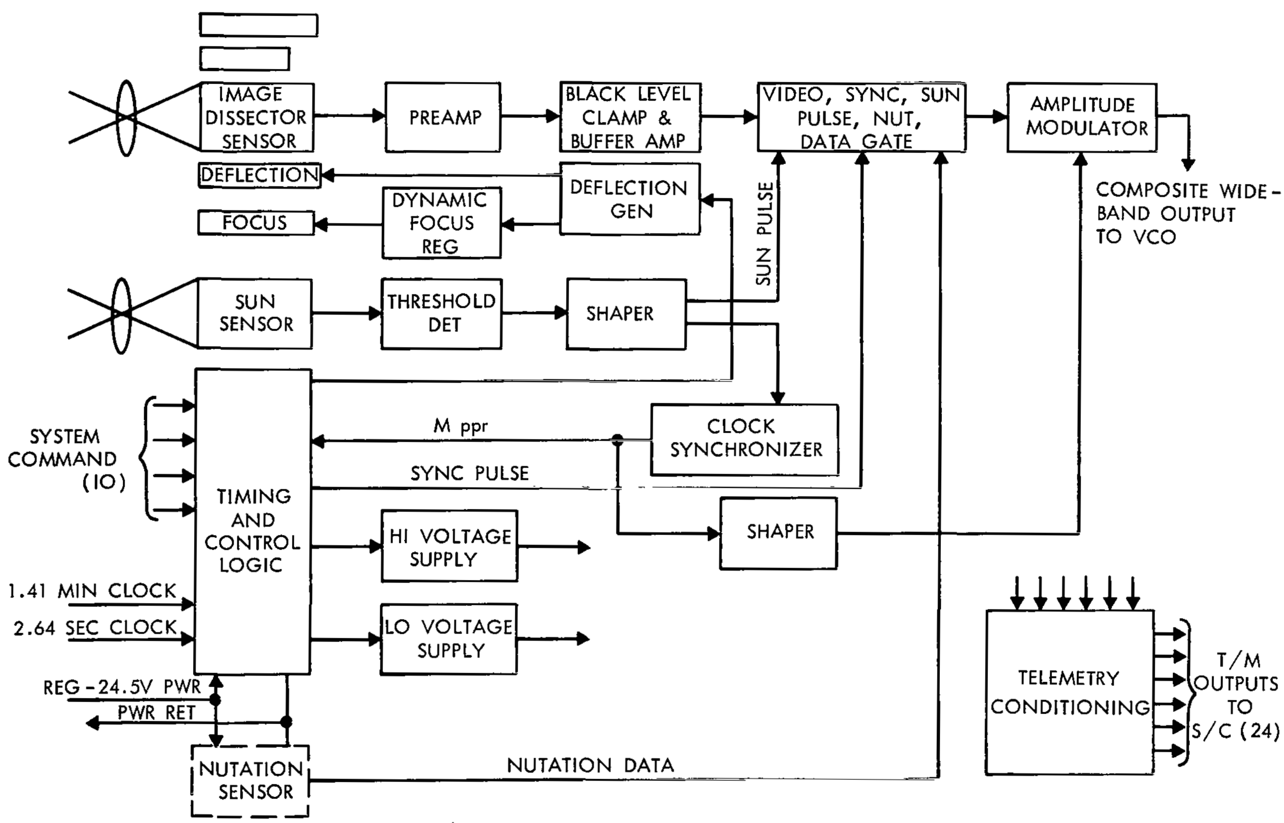

Figure 5—IDC block diagram.

is followed by pulse shapers that provide a pulse of less than one microsecond to the logic circuits and clock synchronizer and an extended pulse to the composite data gate.

The nutation sensor (shown as a dotted line block in Figure 5) mounted physically on the camera but electronically independent, supplies satellite spin-axis nutation data to the camera. At the ground station these data are used to correct nutation-caused errors in the video information.

Sensor

The IDC sensor is 1 inch in diameter and 6-1/2 inches long. A diagram of an image dissector tube is shown in Figure 7. Since the camera is a line-scan device, the tube contains a slit photocathode. A scene is optically focused on the photocathode, which is formed by deposit on the back side of the sensor faceplate. Photoelectrons are emitted from this photoemissive surface in proportion to the light falling on it. The photoelectrons are accelerated toward and focused on a plane parallel to the photocathode. This plane (aperture plane) contains a pinhole aperture at its center. In the IDC tube this aperture is 0.0007 inch in diameter. External magnetic deflection coils deflect the electron image past this aperture. After the electron beam enters the aperture, the secondary-emission electron multiplier section amplifies the video signal by about 10^6. With a photocathode sensitivity of 30 microamps per lumen, this yields a sensor output current of 20 to 35 microamps at scene highlight (10,000 foot-lamberts).

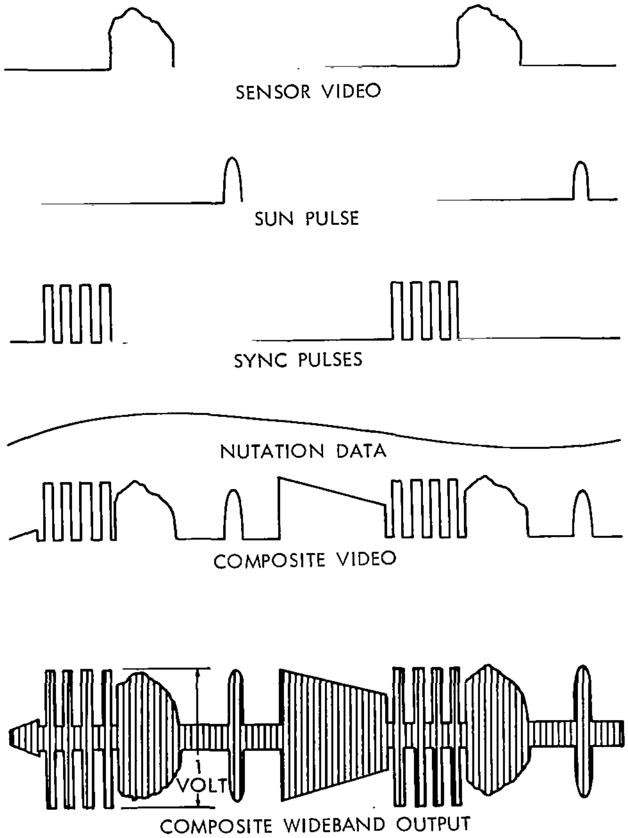

Figure 6—IDC wideband output waveform.

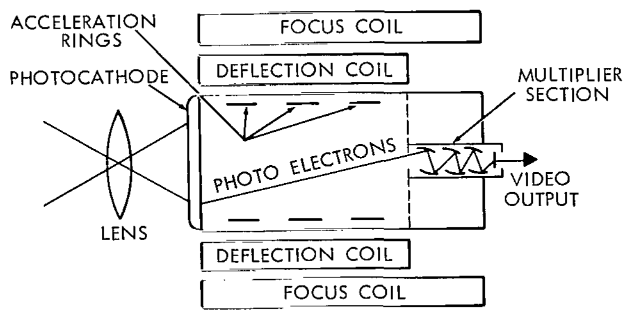

Figure 7—Typical image dissector tube.

Timer and Control Logic

Although the clock synchronizer generates a master clock rate (M clock) proportional to the satellite spin speed, no attempt is made to synchronize camera sweep and timing operations with satellite spin position. The timing and control logic provides a means of attaining and maintaining this synchronization, and also supplies the sync and gating pulses for proper camera output format, proper interface, and routing for the system commands.

Because the satellite is to be earth-synchronous, the delay between the sun sensor viewing the sun and the camera viewing the earth changes by 15 seconds of arc per second of time. The camera system uses the output pulse from the sun sensor as a timing reference. The camera logic must therefore be programmed for the proper delay between sun pulse and earth viewing at initial turn-on, and the change in delay corrected for by the timing and control logic to maintain proper camera operation.

Figure 8 is a block diagram of the timing and control logic. When commanded from the ground by transmission of Frame Start Manual or Frame Start Automatic, the frame control logic generates a frame sync pulse and enables the succeeding sun pulse through to the M + 1 counter. The sun pulse shifts the contents of the Time-of-Day (TOD) counter into the M + 1 counter and allows the M clock through to advance the counter. The contents of the TOD counter are set by Phase Angle Adjust commands to provide the proper delay between sun pulse and camera earth viewing (see above). The TOD counter, 2.64-second clock input, and ramp generator continually adjust for the change in sun pulse to earth-viewing delay. This function will be discussed later in the text. Synchronization outputs are derived from the M + 1 counter by the N and N + S gates. Each of

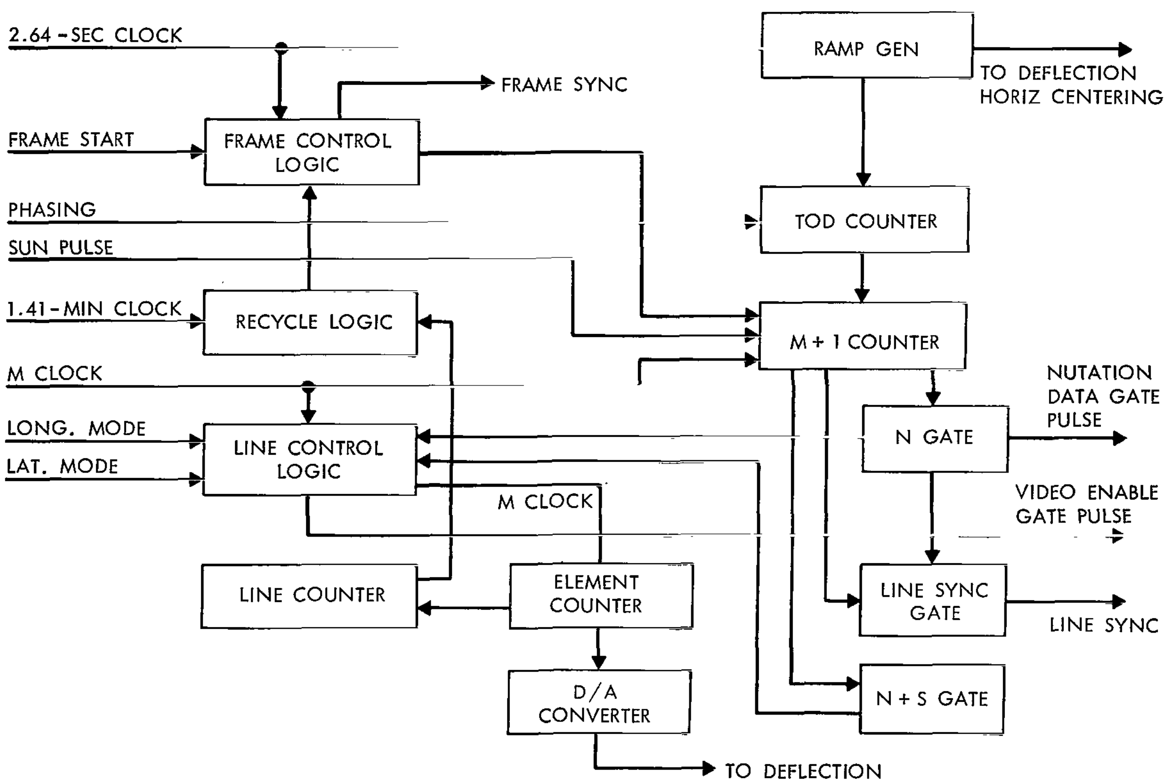

Figure 8–Timing and logic control block diagram.

these synchronization outputs occur once every M + 1 periods of the M clock. Since the M clock period is equal to the time required for the satellite to rotate through one camera resolution element, and since there are M pulses per satellite rotation, a synchronization pulse occurs once for every satellite rotation plus one resolution element.

Figure 9 is a timing diagram of the various logic pulses. In the diagram, t_0 is the time when the line sweeps are initiated. At t_0 minus 48 M-clock periods, the M + 1 counter output enables the N gate. In its enabled state the N gate allows 8 periods of M/2 clock from the M + 1 counter through to the line sync gate. These clocking pulses form the camera line sync output. Following the 8-pulse line sync train, which requires 16 M-clock periods, the N gate remains in the enabled state for 32 more M-clock periods. At t_0 the N gate is returned to its initial state by the M + 1 counter.

The logic circuits described above operate identically in either the primary (longitudinal) or secondary (latitudinal) scanning mode. In the primary scanning mode the trailing edge of the N pulse at t_0 sets the line control logic to let through the M-clock pulse to step the element counter and enable camera video gate. The element counter drives the D/A converter which generates the line sweep deflection waveform. At the count of 1328, the element counter advances the line counter by one, disables camera video from the composite output, enables nutation data to the composite output, and resets the line control logic. At every $t_0 - 48$ pulse from the M + 1 counter, the

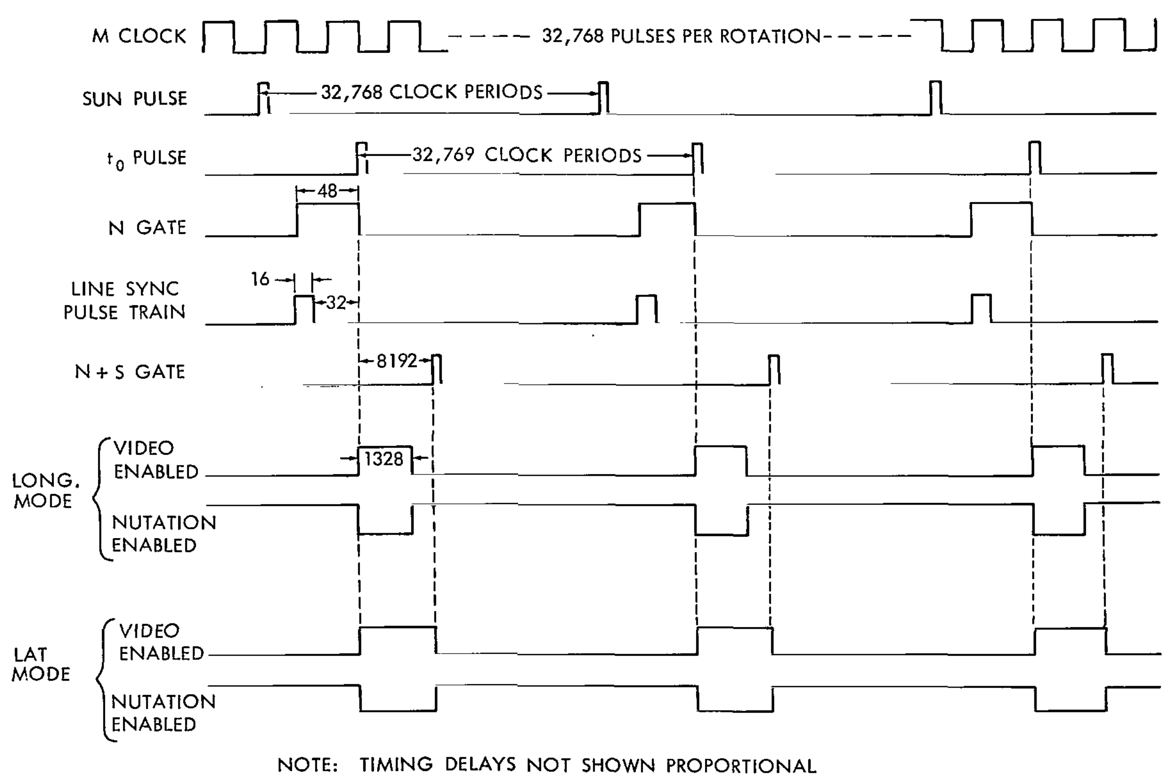

Figure 9—Timing diagram.

logic sequence repeats at an M + 1 rate, until the line counter reaches a count of 1328. Then, if the camera is in the Frame Start Manual mode, the output pulse from the line counter returns it to the standby mode; if the camera is in the Frame Start Automatic mode, the pulse enables the recycle logic to initiate another start pulse to the frame control logic.

In camera operation in the secondary scanning mode, the N + S gate output pulse at t_0 + 8192 M-clock intervals advances both the element and line counters. In this manner the camera sweeps are deflected one resolution element per satellite spin. The N + S gate output also disables camera video and passes nutation data through to the composite output. When the line counter reaches a count of 1328, the camera recycles or shuts down as in the primary scanning mode.

Both camera scanning modes require TOD correction. The 2.64-second clock signal, acting on the ramp generator and TOD counter, makes these corrections. (The camera system resolution element size and the rotational rate of the earth are so related that the change in delay between sun pulse and camera earth viewing is one camera resolution element every 2.64 seconds.)

Line-to-line corrections are made by applying a compensating ramp function to the camera sweeps and an up count of one to the M + 1 counter at intervals of approximately 2.64 seconds. (Approximately, because the up count is not allowed to occur during the earth-viewing or active video period.) The ramp generator provides a compensating skew on the face of the image dissector sensor of one resolution element every 2.64 seconds. The 2.64-sec clock signal recycles the ramp to its initial or no-correction position when the M + 1 counter is advanced by one count. Since the counter corrections are not allowed during active video, this combination provides a smooth and continuous sun-angle delay change or TOD correction. The 2.64-second clock pulse is shaped and phased with the M clock in the clock shaper and phaser to preclude simultaneous occurrence of the 2.64-second correction pulse and the M clock pulse.

Frame-to-frame TOD correction is provided by advancing the TOD counter by one count every 2.64 seconds. This updating of the TOD counter occurs continuously when the camera is in either the operating or standby mode. The contents of the TOD counter are shifted into the M + 1 counter at the beginning of each picture-taking cycle. This updating ensures proper look-angle phasing at the beginning of each picture if the camera is not turned off between pictures. The stability of the satellite 2.64-second clock holds the camera pointing error to less than 1 degree over a 12-hour operating period.

Clock Synchronizer

The clock synchronizer must maintain a system clock rate proportional to the satellite spin speed with an accuracy of 3 parts in 10^6. The problem of maintaining this clock rate is compounded by the wide range of satellite spin speed (60 to 140 rpm) and by a jitter (peak pulse-to-pulse, about 1 part in 10^5) in the sun pulse which supplies the spin rate input to the synchronizer. The digital feedback system described below can satisfy all the IDC system requirements. This system supplies a clock output equal to the satellite spin speed (in revolutions per second) times the number of camera system resolution elements in one satellite rotation. That is, the period between clock pulses equals the time required for the satellite to spin through the portion of a rotation corresponding to one camera system resolution element. In this manner the clock generates 1328 pulses as the camera optical axis passes through its full field of view (14.6 degrees of arc).

Figure 10 is a block diagram of the clock synchronizer. The basic principle around which this phase-locked system has been designed is that of dividing the source frequency F by a fixed integer M to obtain an integer quotient R plus some remainder and then using this remainder as an error source to eliminate itself such that F = MR over the sampling period.

Synchronizer operation is as follows. The M and R counters are initially reset by a sun pulse. At the next sun pulse the contents of the M counter are sensed. If the remainder exceeds the system error threshold (determined by the amount of sun pulse jitter, reference voltage stabilities, system requirements, etc.), the error sense and correction logic delivers one up- or down-count signal to the up/down counter. This counter then drives the digital-to-analog (D/A) converter one unit correction step in the prescribed direction. The output of the D/A converter then drives the VCXO one unit correction step in frequency in the direction dictated by the sensed error. The magnitude of the unit correction step is also determined by the system requirements and capabilities. Each time a correction is made, the M and R counters are reset and the sequence is repeated. This sequence continues until no corrections are required on a rotation-to-rotation or sun-pulse-to-sun-pulse basis. When the error sensed at the receipt of successive sun pulses does

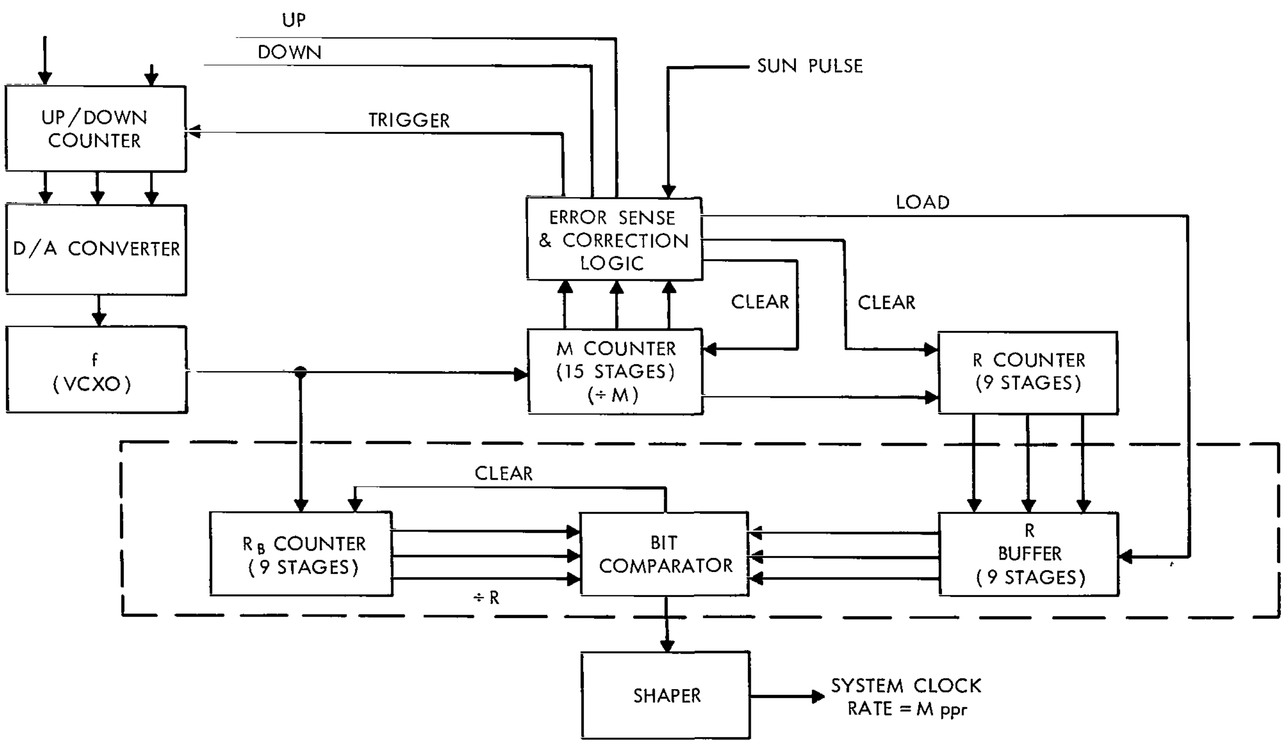

Figure 10–IDC clock synchronizer block diagram.

not exceed the system error threshold, the M counter is not reset. The error or remainder present in the M counter at the receipt of each successive sun pulse accumulates until the error threshold is exceeded; then, the correction and reset process repeats. The feedback portion of the synchronizer acts as an error integrator and makes corrections only as often as is necessary to retain lock. It should be noted that corrections are made in unit correction steps regardless of how much the system clock is out of lock. The error threshold has been chosen as plus and minus 5 resolution elements, and the unit correction step as approximately 1/10 of a resolution element.

The divide-by-R block in Figure 10 (shown in dotted lines) operates as follows. The contents of the R counter are parallel-shifted into the R buffer at the receipt of each sun pulse. The R buffer, bit comparator, R_B counter combination then divide F by that number (R). Since F = MR over one spin period after the system is locked in, the output of the system is M pulses per spacecraft rotation. Thus, M is the number of resolution elements in a full satellite rotation. For this system, M is 32,768, F is 10.789 MHz ± 80 kHz, and R can take on values of from 329 to 140 at 60 and 140 rpm respectively.

GROUND SUPPORT EQUIPMENT

The primary display equipment for the IDC Experiment will be located at NASA's Goddard Space Flight Center. The composite video information will be received from the satellite at the Rosman, N. C., facility and transmitted to Goddard via wideband transmission lines. A block diagram of the ground support complex is shown in Figure 11. The tape recorders will be available at both Rosman and Goddard to allow both real-time and off-line data reduction and display. All portions of the ground support equipment except the video demodulator-sync generator can be used to record, transmit, or display video information from various types of camera systems. The photofax display unit can display video information with resolutions of up to 2048 TV lines.

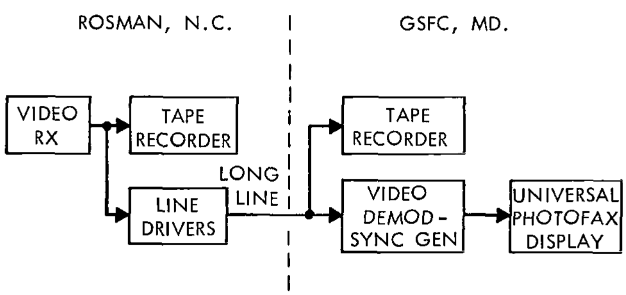

Figure 11—Ground station general block diagram.

Video Demodulator-Sync Generator

The video demodulator-sync generator portion of the ground station is shown in Figure 12. The purpose of this unit is to supply line sync, frame sync, deflection clocking, and video information to the photofax display. The system also provides automatic correction of satellite nutational pointing errors in the video information. A sun pulse detector is included to allow an alternate output from which satellite spin rate can be determined.

The receiver output (camera composite output amplitude-modulated on the M-clock subcarrier) is connected through the input buffer amplifier to the clock extraction circuits, the line sync detector, and the amplitude demodulator.

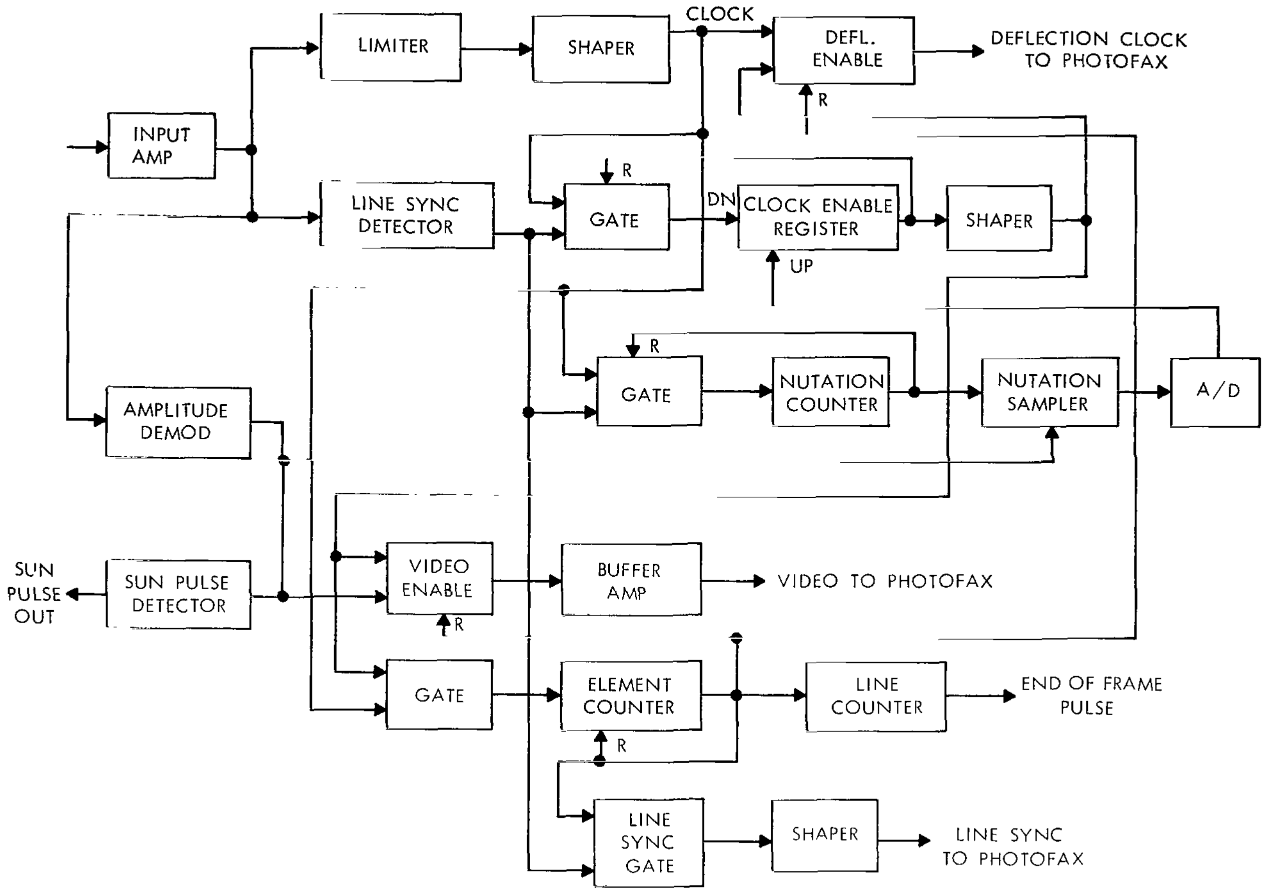

Figure 12–Video demod-sync generator block diagram.

The clock extraction circuits consist of a hard limiter followed by a shaper. The M-clock output is connected, after proper sequence gating, as a driving pulse to the photofax digital deflection circuits. It also clocks the element and nutation counters and the nutation correction logic.

The line sync detector generates an output pulse upon recognition of each line sync pulse train from the camera. This unit also produces an output pulse if the incoming line sync pulse train is not detected by the time the nutation counter indicates that it should be received. The output pulse from the detector initiates the nutation correction sequence and clears the nutation counter.

The nutation counter accumulates at M-clock rate starting from a zero count at t_0 minus 32 camera time, which is the end of line sync. When the number 32704 is detected in this counter, the nutation sampler can sample and hold the level of the demodulated composite video. The sampled dc voltage is converted to a binary number, which is stored in the clock-enable register. When the line sync detector output pulse occurs, the M clock is allowed to count this register back to zero. The pulse generated when this zero is detected passes baseband video to the photofax video amplifiers, the M clock through to the element counter, and the M clock stepping pulses through to the photofax deflection circuits. Since the time at which this enable pulse occurs varies directly with the amplitude of sampled nutation, the time of initiation of photofax line sweep is directly related to nutation level. Camera pointing errors introduced by satellite nutation are such that this variation of line sweep initiation timing corrects for the longitudinal components of these errors. The system can make corrections up to ±16 camera resolution elements.

The element counter is sensed for a count of 1364, which ensures a full line sweep by the photofax regardless of nutation correction, at which time the video and deflection clock gates are inhibited and the line counter is advanced by one count. When the line counter reaches a count of 1328, an end-of-frame pulse is generated; this resets all logic to initial conditions and actuates an end-of-frame indicator lamp.

The amplitude demodulator contains a variable low-pass filter whose high-frequency cutoff must be adjusted according to the satellite spin rate. This is necessary because the baseband video and subcarrier (M clock) frequencies vary with satellite spin rate and overlap at the extremes of the satellite spin-rate range. That is, the baseband frequency at the fastest spin rate is higher than the subcarrier frequency at the slowest spin rate.

Camera System Testing

During operational tests of the IDC, a spin simulator, which consists of a spinning mirror, a solar lamp, and a target collimator, is used to reproduce as accurately as possible the data format that the camera will see from a spinning satellite. Figure 13 shows a picture taken by the engineering model IDC using this spin simulator. At the time of this writing the flight unit IDC is in the final phases of environmental testing.

Figure 13—Picture taken by IDC using spin simulator.

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